PROGRAMMING FLASH MEMORY VIA A BOUNDARY SCAN REGISTER

CLAIM FOR PRIORITY

This application claims priority to German Application No. 10244757.8, filed September 25, 2002, the contents of which are hereby incorporated by reference.

TECHNICAL FIELD OF THE INVENTION

The underlying invention is based on a method and an interface for on-board programming and/or In-System Configuration (ISC) of flash memory mounted on a printed circuit board by controlling its inputs with the aid of an application-specific integrated circuit mounted on the same circuit board via a Boundary Scan (BSCAN) register of which the outputs are provided for activating or deactivating a write operation.

BACKGROUND OF THE INVENTION

The Boundary Scan technique (BSCAN) is a standardized method for board tests, that was formally approved in 1990 as industry standard IEEE 1149.1 for Test Access Port (TAP) and Boundary Scan (BSCAN) architectures. Connection tests at board level in the production of complex printed circuit boards (PCBs) are based on this specification. If the test object has its own microprocessor as well as flash-based program memory, a built-In self test can be implemented for example by loading the flash memory via Boundary Scan with the aid of a self-test program. Test results stored in memory can be read out again by Boundary Scan after the ending of the test procedure in this case.

To execute Boundary Scan tests two conditions must be fulfilled: At least a few of the integrated circuits (ICs) on the board must comply with the BSCAN specification. In the

testing test vectors will then be used to have the desired test executed by a BSCAN register. In addition the product developers must provide a scan path between the individual ICs which leads from the Test Access Port (TAP) through the ICs back to the TAP where the data is finally scanned. For testing electrical connections Boundary Scan tests represent an excellent alternative to in-circuit tests (ICTs). The costs of performing function testing are low, and because of the increasing miniaturization of integrated semiconductor components the assumption is that the trend towards boundary scan will continue.

IEEE-Standard 1149.1 specifies both the necessary hardware structures and also a suitable form of description of all these characteristics in the form of the Boundary Scan Description Language (BSDL). In this case, this standard is kept so open that by definition of customer-specific registers and corresponding instructions application-specific functions can be implemented without losing compatibility. This is precisely the basic premise on which all conventional procedures for in-system programming (ISP) of integrated ASICs which operate on the basis of Boundary Scan are also based, but to date no standard for this has existed. Nor is there a uniform definition of test vector formats for data interchange contained in IEEE-Standard 1149.1.

Whereas the Boundary Scan method in accordance with IEEE-Standard 1149.1 was previously primarily used as an innovative technology for function testing of integrated circuits or for verification and simulation of hardware fault functions, the most recent developments show further possible applications of this principle. As well as use for test purposes, Boundary Scan will also be used very effectively in

the area of what is known as In-System-Programming (ISP) of flash memories as well as Programmable Logic Device (PLD) chips, such as Field-Programmable Gate Arrays (FPGAs) with up to 10,000 logic gates per array or Programmable Logic Arrays (PLAs). In this case the individual control and address inputs of a flash memory will be simulated via the chained BSCAN cells of a BSCAN register assigned to these inputs in such a way that either a read or a write operation will be triggered. As can be seen from the basic diagram shown in Fig. 1, the control, address and data signals of the corresponding BSCAN cells can be recorded and output.

IEEE-Standard 1532 published in January 2001 created for the first time a uniform set of standards for the system architecture and a suitable data format for In-System Configuration (ISC) of programmable integrated ASICs. This Standard describes a series of obligatory and optional programming instructions and corresponding data registers. In principle IEEE Standard 1532 represents an expansion of IEEE Standard 1149.1 specifically tailored to the requirements of programming for standardizing the programming process for programmable logic chips, but is fully compatible with the latter. Since IEEE Standard 1532 related exclusively to programmable logic chips however which feature a JTAG interface and are able to store programming data internally, this standard does not relate to flash memory without a JTAG interface. Basically IEEE Standard 1532 includes the standardization of specific ISC data registers, ISC instructions, BSDL expansions for the description of the ISC features as well as a specific file format.

This means that Standard IEEE 1532 goes far beyond all previous solutions and, on the basis of its innovative character,

also allows simultaneous programming of a number of compatible components. By using a series of additional functions, such as the use of special program voltage pins, compliance-enable pins and the possibility of defining optional ISC instructions, IEEE 1532 also offers the necessary scope for creating application-specific compatibilities. With IEEE Standard 1532 this basically involves a methodical separation of process information and programming files.

The component information needed for programming is contained in corresponding "BSDL expansions" of a BSDL file. A quite major component from the user's standpoint here is what is known as the "Attribute ISC_Flow". This implements the basic programming functions such as Delete, Program, Verify etc., in corresponding test sequences. If a number of IEEE-1532-compatible components are to be programmed simultaneously, the programming software must have the capability to virtually merge any number of "Attribute ISC_Flows". Because of this methodology IEEE Standard 1532 provides the facility for programming PLDs from different manufacturers independent of the process technology (e.g. EEPROM, SRAM or flash-based), their architecture or their voltage level.

The BSDL files must be provided type-specifically by the relevant chip manufacturer. In this regard they are a quite significant part of the delivery scope. By contrast the programming data is created individually by the PLD designer via a corresponding target compiler in the form of a data file. Without going into more detail it should merely be mentioned that this involves ASCII files with a specific syntax so that they can be read and edited. In accordance with this function principle, for each component to be programmed there must be a BDSL file and a data file consistent with it available.

Even if the previously described theory of IEEE Standards 1532 appears to promise much, it is in no way sufficient for the practical success of this Standard. The programming software in particular occupies a key position because of the multiplicity of functions necessary and has a decisive effect on determining the efficiency of the ISC operations.

For simultaneous programming of a number of components the time savings that can be achieved depend on a number of different factors. Particular factors to mention here are the complexity, architecture, technology and clock rate of the component involved. To this extent verifiable quantitative statements also depend on the relevant implementation and application.

With Boundary Scan in particular the continuing development of the software tools plays a decisive role for effective implementation of this trailblazing technology in practice. In conjunction with BSCAN-based on-board programming of flash memories, the prior art in this case is especially the integrated development and programming environment system CASCON ™ from GÖPEL electronic GmbH of Jena.

To combine the new programming methods with other BSCAN procedures such as debugging, production tests or flash programming, GÖPEL provides a J-Drive program engine that is included for In-System Configuration (ISC) of a PLD directly in the Boundary Scan software package system CASCON ™ and POLARIS ™ This J-Drive program Engine accesses configuration data from a BSDL file for configuration of a Test Access Port (TAP) according to IEEE Standard 1149.1 which will be used as a control unit to control the BSCAN cells of the BSCAN regis-

ter via a program interface. In connection with the available controllers based on USB, PCI, PXI or VXI, this allows cost-optimized multi-mode boundary scan systems to be configured with performance tailored for labor, production and service. This makes it possible for example in production to test with just one device a PLD mounted on a circuit board for manufacturing faults, then to configure the PLD and to load a specific production version of the firmware into an available flash memory.

According to the prior art, flash memories are programmed as a rule with the aid of application-specific integrated circuits (ASICs) which are in a position to configure the flash memory involved even during operation. As a rule these are ASICs which support the JTAG Standard IEEE 1149.1 (cf. Fig. 1: Interface between ASIC-1 and Flash-1). For this purpose an abbreviated BSCAN register is used where necessary, with the aid of which the period required for programming the flash memory can be decisively shortened.

However using this method produces a number of problems: Thus for example for programming a flash memory creation of a program is relatively expensive since the configuration (i.e. the connections between ASIC and Flash memory) is taken from the circuit diagram or from the network list derived from it and the BSDL file of the ASIC must be included. Furthermore simultaneous programming of a number of integrated semiconductor components mounted on the same circuit board is not currently possible. Above and beyond this, with conventional methods burst mode is also not possible since with each write cycle the programming data has to be shifted into the ASIC as well as the addresses and the control bits too as a rule.

SUMMARY OF THE INVENTION

The present invention provides a method of on-board programming as well as In-System Configuration (ISC) of flash memory by stimulating individual of its inputs via memory cells of a BSCAN register to activate or deactivate a write operation, for which application the circuit diagram needed for on-board programming or the network list derived from it no longer needs to be included.

Furthermore simultaneous programming of a number of flash memories mounted on the same circuit board should also be made possible, even in burst mode.

In one embodiment of the invention, there is a method as a well as a parallel interface for on-board programming and/or In-System Configuration(ISC) of a flash memory mounted on a printed circuit board is provided by controlling individual inputs of the flash memory with the aid of an application-specific integrated circuit mounted on the same circuit board via individual memory cells of a BSCAN register to activate or deactivate a write operation. In this case, the architecture description of the ASIC and of the flash memory to be programmed as well as the data format of the program (DATA_IN) and configuration data (Conf data) are stored in a BSDL file. The circuit board can be controlled via a JTAG interface for input or output of standard bus signals (TDI, TDO, TMS, TCK and TRST) suitable for performing function testing of the flash memory as well as for input of the control signals of the ASIC.

To reduce the programming effort, in accordance with the invention, the data of the circuit diagram or of the network list derived from it, which defines the configuration of the

interface between the flash memory to be programmed and the ASIC, is stored in a further file (BSDL file) so that the flash memory to be programmed, after adaptation of the features of the flash memory to IEEE Standard 1532 can be programmed via a JTAG interface in the same way as a programmable logic device (PLD).

BRIEF DESCRIPTION OF THE DRAWINGS

Further features, characteristics, benefits and applications of the underlying invention are described in the following description of exemplary embodiments of the invention which are shown in Figs. 1 to 3. The diagrams show:

Fig. 1 Shows a circuit layout of a Printed Circuit Board (PCB), which is suitable for programming and configuration of two flash memories via a Boundary Scan (BSCAN) register via a JTAG interface according to Standard IEEE 1532, whereby the interface between the ASIC and the second flash memory is formed by a part of the BSCAN register.

Fig. 2 shows a reduced circuit layout of the same PCB for programming and configuration of an integrated flash memory via a BSCAN register via a JTAG interface based on a BSDL file according to Standard IEEE 1532, whereby a configuration register according to IEEE Standard 1532 is connected to the output of an application-specific integrated circuit.

Fig. 3 shows detailed views of two exemplary embodiments of the circuit layout for connecting the multiplexes and flip-flops of a scan cell of the BSCAN register and a capture cell of the configuration

register for provision of the control, data and address signals needed for programming the flash memory.

DETAILED DESCRIPTION OF THE INVENTION

The invention is explained in more detail below using the exemplary embodiments illustrated in Figures 1 to 3. The meaning of the symbols provided with reference numbers in Figs. 1 to 3 can be taken from the enclosed list of reference numbers.

Within the context of an exemplary embodiment of the present invention there is provision for an ASIC 108, suitably adapted for on-board programming and In-System Configuration (ISC) of a flash memory 116, which can be controlled via a JTAG interface 102 in accordance with IEEE Standard 1149.1 and reprograms or configures the flash memory 116 even during operation. In accordance with the invention, ASIC 108 and flash memory to be programmed 116 are considered with the context of IEEE Standard 1532 as contiguous unit 120 (see FIG. 1 and 2). As a result it makes no difference whether flash memory 116 is inside or outside ASIC 108.

If one gives this ASIC 108 characteristics in accordance with IEEE Standard 1532, the flash memory 116 can be programmed in the same way as a programmable logic device (PLD). In this case, the data of the circuit diagram or of the network list that can be derived from it which defines the configuration of interface 118 and 119b between flash memory to be programmed 116 and ASIC 108 is stored in the BSDL file. The benefits of this are as follows:

- Since the BSDL file now includes information for programming flash memory 116 the circuit diagram or the network lists derived from it no longer have to be included for program creation. Thus the programming algorithm, as with programmable logic devices (PLDs) can be generated automatically by JTAG tools, such as the BSCAN software package system CASCON ™ from GÖPEL electronic GmbH.

- Further simultaneous programming and/or configuration of a number of ASICs 114, 116 mounted on the same circuit board 100 is possible, which means that even during production of the circuit board 100 a significant cost reduction can be achieved.

- Over and above this the underlying invention also makes possible, after connection of a configuration register 119b for buffering address and control data that occur at the outputs of the ASIC 108 provided for programming the flash memory 116, the programming or configuration of the flash memory 116 in burst mode.

IEEE-Standard 1532 allows a number of options for provision of control, data and address information via JTAG interface 102. In an exemplary embodiment of the present invention the "Memory Array" of a PLD specified in accordance with IEEE Standard 1532 which includes the configuration data which defines the programmed functions of the PLD is replaced by a parallel interface 118, 119b (external Memory Array) to an external flash memory 116. This in its turn offers a number of options:

- The parallel interface between the ASIC 108 and the flash memory to be programmed 116 will be formed by connecting in

series a number of memory cells 204a which are part of the BSCAN register 118 (see Fig. 1).

- Alternatively, a configuration register 119b suitably adapted for In-System Configuration (ISC) of the flash memory to be programmed 116, such as one of the ISC_PData or ISC_ RData registers specified according to IEEE Standard 1532 can be connected to the outputs of ASIC 108 as a parallel interface between ASIC 108 and the flash memory to be programmed 116 (see Fig. 2). As shown in Fig. 3, the option of three different connections is then possible:

  a) connecting the control, data and/or addressing inputs of the flash memory to be programmed 116 to ASIC 108 (normal mode),

  b) connecting the control, data and/or addressing inputs of the flash memory to be programmed 116 to a signal input for BSCAN test data (SCAN_IN) for function testing of the flash memory, or

  c) connecting the control, data and/or addressing inputs of the flash memory to be programmed 116 with the configuration register 119b for configuration of the flash memory with the aid of the configuration data stored in the BSDL file.

This is achieved by modification of BSCAN cell 204, as shown in Fig. 3. In accordance with the invention, this type of BSCAN cell 204 has an input multiplexer 302a for switching a through connection of one of at least two input signals (DATA_IN, SCAN_IN) depending on a control signal (SHIFT_DR) present at a control signal input (SEL) which allows the op-

tion of a connection from ASIC 108 or from a signal input for BSCAN test data (SCAN_IN) to flash memory 116. A scan or capture flip-flop 304 is used to buffer the programming data received from ASIC 108 (DATA_ IN) or the BSCAN test data (SCAN_IN). For initiating or ending a write operation an update flip-flop 306 is used, with the aid of which individual control signals, data and/or address inputs of the flash memory 116 are controlled. Via an output multiplexer 302b1 or 302b2 for through connecting one of at least two input signals (DATA_IN, SCAN_ OUT, conf data), depending on a control signal (MODE) present at a control signal input (SEL), there is the option of switching through a connection from ASIC 108 or from a signal input for configuration data (Conf data) to flash memory 116.

A scan or capture cell 204a of configuration register 119b for In-System Configuration (ISC) of Flash memory 116 consists in accordance with the first exemplary embodiment of the present invention of a scan or capture flip-flop 308 for buffering the data received from ASIC 108 (Conf data) and an output multiplexer 302c for through connecting one of two input signals (SCAN_OUT, Conf data) depending on a control signal (UPD_DR) present at a control signal input (SEL). This gives the option of switching a connection from ASIC 108, from a signal input for BSCAN test data (SCAN_IN) or from a signal input for configuration data (Conf data) through to flash memory 116.

In accordance with a second exemplary embodiment of the present invention, instead of output multiplexer 302c an update flip-flop 306 is used for controlling individual control signal, data and/or address inputs of flash memory 116 in order to trigger or end a write operation.

The decisive advantage of the present invention over conventional methods of on-board programming according to the prior art lies in the fact that with the aid of the method in accordance with the invention the differences between flash and PLD programming are eliminated. In this case, ASIC 108 and flash memory 116 form one unit within the context of IEEE Standard 1532. The fact that the circuit characteristics are stored in the BSDL file also gives the user the benefit of a significant reduction in programming effort, since the connections between ASIC 108 and flash memory 116 no longer have to be taken from the circuit diagram or from the network lists derived from it.